**Shailendra Yadav**

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**CAREER VISION**

Seeking position to utilize my skills and abilities in the information technology industry that offer professional growth while being resourceful, innovative and flexible.

Entry level position in Software Design / Development.

**TECHNICAL SUMMARY**

* **JAVA**
* Good knowledge of OOPs concept like Abstraction, Encapsulation, Polymorphism, Inheritance.
* Good knowledge of strings.
* Good in Exception handling and written custom exception.
* Good practical knowledge of Collections, Framework and Data Structure like List, Set, Map and Queue etc.
* Implemented custom sorting using comparable and comparator.
* **SQL**
* Good understanding of RDBMS concepts.
* Comfortable in writing SQL statements like DDL, DML, DQL etc.
* Implemented Joins and Subqueries.
* **HTML**
* Good understanding of basics of coding and markup language.
* Good understanding of creating HTML forms.
* Good understanding of creating HTML layouts.
* Good understanding of HTML 5 tags.
* **CSS**
* Good understanding styling tags.
* Good understanding of selectors.
* Good understanding of HTML Formatting.
* **JAVASCRIPT**
* Good understanding of Basics of JavaScript
* Good understanding of API projects.
* Good understanding of BOM and DOM concepts.

**GIT-HUB LINK**

* <https://github.com/YaduwanshiShailendra>

**TECHNICAL SKILLS**

* **Programming**: Java, SQL, PL/SQL
* **Web Technology:** HTML, CSS, Basics of JAVASCRIPT, Basics of Angular
* **RDBMS:** Oracle, MY-SQL
* **Tools / IDE:** Eclipse, SQL Developer, VS Code, Sublime Text, MySQL, SQL-Yog, Oracle 10g.
* **OS:** Windows, Unix

**CERTIFICATIONS**

* Completed (**JAVA, SQL & Web Technologies**) Training from Jspiders BTM Bangalore.
* Completed **Embedded System Design** Training from CRISP, Bhopal.
* Completed **PLC Application & Networking** Training from CRISP, Bhopal.
* Completed **Broadcasting** Training from various centers of All India Radio, Bhopal.

**EDUCATIONAL QUALIFICATION**

* **M.Tech**- Completed M.Tech in Embedded System & VLSI Design from Vidhyapeeth Institute of Science & Technology, Bhopal in 2017 with CGPA of 7.6.
* **B.E**- Completed B.E in Electronics and Communication from Trinity Institute of Technology & Research, Bhopal in 2013 with aggregate of 68.28%.
* **12th** from Dynamic Public School, Bhopal in 2009 with percentage of 65.60 %. M.P. Board.
* **10th** from Ideal Higher Secondary School, Bhopal in 2006 with percentage of 66.40 %. M.P. Board.

**PROJECTS**

* **Postgraduate Thesis, VIDHYAPEETH INSTITUTE OF SCIENCE & TECHNOLOGY, BHOPAL, India 2017.**

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| **AIM** | Power Efficient 16-Bit Shift Register Using GDI Based Delayed Pulsed Generator & Dual Edge Latch In 35nm Technology. |
| **Tool** | TANNER EDA v16.0 |
| **Description** | The objective of this project is to implement a 16-bit shift register using latches and delayed clock pulse generator with Vdd=0.3V and simulation is done by using Tanner EDA v16.01 Tool in 35 nm CMOS technology. |

* **Undergraduate Project, TRINITY INSTITUTE OF TECHNOLOGY & RESEARCH, BHOPAL, India 2013.**

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| **MAJOR PROJECT** | OFDM SIMULATION In MATLAB |
| **Team Size** | Four |
| **Tool** | MATLAB |
| **Description** | The objective of this project is to demonstrate the concept and feasibility of an OFDM system, and investigate how its performance is changed by varying some of its major parameters. |
|  |  |
| **MINOR PROJECT** | MOBILE DETECTOR |
| **Team Size** | Four |
| **Tool** | Tina Pro |
| **Description** | This is a mobile phone sniffer circuit that can detect the signal being used in GSM band (about 900 MHz). It can detect only the signal activity not the message content through headphone. |

**TECHNICAL PAPERS AND WORKSHOPS**

* Delayed clock pulse triggered modified latch low power shift register using G.D.I. Technique, published in International Journal of Scientific Progress & Research (IJSPR) Vol-25, 2016.
* Power efficient 16-bit Shift Register using G.D.I. based delayed pulse generator and dual edge latch in 35nm technology, published in International Journal of Innovative Research in Computer & Communication Engineering (IJIRCCE) Vol-4, issue-8, 2016.
* Ethical hacking workshop by Ankit Fadia conducted in T.I.T.R.
* Participated in seminar of Dream Spark Yatra conducted by Microsoft in T.I.T.R. in 2011.

**PERSONAL STRENGTH**

* Quick learner of new things and hard working and enthusiastic.
* If any of task assigned, would like to take responsibility as an initiative.
* Co-operative with others at work and ability to deal with people diplomatically.

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**Place:** Bangalore

**Date:**  07/08/2020 (Shailendra Yadav)